AMENDMENTS TO THE CLAIMS:

Please amend claims 1, 5, 9, 11, 15, 19 and 21 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A data processing apparatus, comprising:

a processor operable to execute a stream of instructions;

a prefetch unit operable to prefetch instructions from a memory prior to sending those instructions to the processor for execution, the prefetch unit being operable to receive from the memory simultaneously a plurality of prefetched instructions from sequential addresses in memory, and being operable to detect whether any of those prefetched instructions are an instruction flow changing instruction, and based thereon to output a fetch address for a next instruction to be prefetched by the prefetch unit; ~~and~~

address generation logic, within the prefetch unit and ~~operable, for~~responsive to a selected prefetched instruction that is detected to be said instruction flow changing instruction, ~~to determine~~for determining a target address to be output as the fetch address, the address generation logic having a first address generation path ~~operable to determine~~for determining the target address if the selected prefetched instruction is a first prefetched instruction in said plurality, and at least one further address generation path ~~operable to determine~~for determining the target address if the selected prefetched instruction is one of the other prefetched instructions in said plurality, the first prefetched instruction being earlier in said stream than said other prefetched instructions, the first address generation path ~~being arranged to generate~~generating the target address more quickly than the at least one ~~other~~further address generation path; and

a pipeline stage, provided in said at least one further address generation path, for increasing generation speed of the target address by the first address generation path, whereby, in the event that the first prefetched instruction is said selected prefetched instruction, the prefetch unit ~~is operable to~~ outputs the associated target address as the fetch address earlier than if one of said other prefetched instructions is said selected prefetched instruction.

2. (original) A data processing apparatus as claimed in Claim 1, further comprising:

prediction logic operable to predict, for a prefetched instruction whose execution is conditional, whether that conditional prefetched instruction will be executed by the processor;

in the event that the first prefetched instruction is said selected prefetched instruction and its execution is conditional, the prefetch unit being operable to output the associated target address as the fetch address if the prediction logic predicts that the first prefetched instruction will be executed by the processor.

3. (original) A data processing apparatus as claimed in Claim 1, wherein the prefetch unit associates a different priority level with each of the plurality of prefetched instructions, the first prefetched instruction having the highest priority level, and if more than one of the plurality of prefetched instructions is detected to be said instruction flow changing instruction, the prefetch unit is operable to determine as said selected prefetched instruction the prefetched instruction having the higher priority level from those prefetched instructions detected to be said instruction flow changing instruction, whereby the target address associated with that selected prefetched instruction is output as the fetch address.

4. (original) A data processing apparatus as claimed in Claim 1, wherein the address generation logic is operable to generate the target address for the first prefetched instruction in a same clock cycle as the prefetch unit detects that that first prefetched instruction is said instruction flow changing instruction.

5. (currently amended) A data processing apparatus as claimed in Claim 1, wherein predetermined logic is shared between the first address generation path and the at least one further address generation path~~, and a pipeline stage is provided in the at least one further address generation path in order to increase speed of generation of the target address by the first address generation path~~.

6. (original) A data processing apparatus as claimed in Claim 1, wherein the at least one further address generation path comprises a single further address generation path used to determine the target address for any prefetched instructions other than said first prefetched instruction.

7. (original) A data processing apparatus as claimed in Claim 1, wherein the prefetch unit comprises decode logic operable to detect whether any of the plurality of prefetched instructions are said instruction flow changing instruction, the decode logic further being operable to decode from each prefetched instruction detected to be said instruction flow changing instruction an immediate value to be input to the address generation logic.

8. (original) A data processing apparatus as claimed in Claim 7, wherein the address generation logic comprises adder logic operable to determine the target address for the selected

prefetched instruction by adding the associated input immediate value to the address of that selected prefetched instruction.

9. (currently amended) A data processing apparatus as claimed in Claim 8, wherein the adder logic is shared between the first address generation path and the at least one further address generation path~~, and a pipeline stage is provided in the at least one further address generation path in order to increase speed of generation of the target address by the first address generation path~~.

10. (original) A data processing apparatus as claimed in Claim 1, wherein if none of the plurality of prefetched instructions is said instruction flow changing instruction, the prefetch unit is operable to generate the fetch address by incrementing a previous fetch address output by the prefetch unit.

11. (currently amended) A method of operating a data processing apparatus to determine a target address for an instruction flow changing instruction, the data processing apparatus having a processor operable to execute a stream of instructions, and a prefetch unit operable to prefetch instructions from a memory prior to sending those instructions to the processor for execution, and to output a fetch address for a next instruction to be prefetched from the memory, the method comprising the steps of:

(a) receiving from the memory simultaneously a plurality of prefetched instructions from sequential addresses in memory;

(b) detecting whether any of those prefetched instructions are an instruction flow changing instruction; and

(c) for a selected prefetched instruction that is detected to be said instruction flow changing instruction, determining a target address to be output as the fetch address by performing one of the steps of:

(c)(1) employing a first address generation path to determine the target address if the selected prefetched instruction is a first prefetched instruction in said plurality; or

(c)(2) employing at least one further address generation path to determine the target address if the selected prefetched instruction is one of the other prefetched instructions in said plurality;

the first prefetched instruction being earlier in said stream than said other prefetched instructions, and the first address generation path being arranged to generate the target address more quickly than the at least one ~~other~~further address generation path; ~~and~~

(d) providing a pipeline stage in the at least one further address generation path in order to increase speed of generation of the target address by the first address generation path; and

(e) outputting as the fetch address the target address generated at step (c);

whereby, in the event that the first prefetched instruction is said selected prefetched instruction, the prefetch unit is operable to output the associated target address as the fetch address earlier than if one of said other prefetched instructions is said selected prefetched instruction.

12. (original) A method as claimed in Claim 11, further comprising the step of:

employing prediction logic to predict, for a prefetched instruction whose execution is conditional, whether that conditional prefetched instruction will be executed by the processor;

in the event that the first prefetched instruction is said selected prefetched instruction and its execution is conditional, the prefetch unit being operable to output the associated target address as

the fetch address if the prediction logic predicts that the first prefetched instruction will be executed by the processor.

13. (original) A method as claimed in Claim 11, further comprising the steps of:

associating a different priority level with each of the plurality of prefetched instructions, the first prefetched instruction having the highest priority level;

if more than one of the plurality of prefetched instructions is detected to be said instruction flow changing instruction, determining as said selected prefetched instruction for said step (c) the prefetched instruction having the higher priority level from those prefetched instructions detected to be said instruction flow changing instruction;

whereby at said step (d) the target address associated with that selected prefetched instruction is output as the fetch address.

14. (original) A method as claimed in Claim 11, wherein at said step (c)(1) the target address for the first prefetched instruction is generated in a same clock cycle that, during said step (b), that first prefetched instruction is detected as said instruction flow changing instruction.

15. (currently amended) A method as claimed in Claim 11, wherein predetermined logic is shared between the first address generation path and the at least one further address generation path~~, and the method further comprises the step of:~~

~~providing a pipeline stage in the at least one further address generation path in order to increase speed of generation of the target address by the first address generation path~~.

16. (original) A method as claimed in Claim 11, wherein the at least one further address generation path comprises a single further address generation path used at said step (c)(2) to determine the target address for any prefetched instructions other than said first prefetched instruction.

17. (original) A method as claimed in Claim 11, wherein the prefetch unit comprises decode logic operable at said step (b) to detect whether any of the plurality of prefetched instructions are said instruction flow changing instruction, the method further comprising the step of:

employing the decode logic to decode from each prefetched instruction detected to be said instruction flow changing instruction an immediate value for use in said step (c).

18. (original) A method as claimed in Claim 17, wherein at said step (c) the target address for the selected prefetched instruction is determined by adding the associated immediate value to the address of that selected prefetched instruction.

19. (currently amended) A method as claimed in Claim 18, wherein adder logic used to perform said adding step is shared between the first address generation path and the at least one further address generation path~~, the method further comprising the step of:~~

~~providing a pipeline stage in the at least one further address generation path in order to increase speed of generation of the target address by the first address generation path~~.

20. (original) A method as claimed in Claim 11, wherein if none of the plurality of prefetched instructions is determined at said step (b) to be said instruction flow changing instruction, the method further comprises the step of:

generating the fetch address by incrementing a previous fetch address output by the prefetch unit, and outputting that fetch address at said step (d).

21. (currently amended) A prefetch unit for a data processing apparatus that has a processor operable to execute a stream of instructions, the prefetch unit being operable to prefetch instructions from a memory prior to sending those instructions to the processor for execution, the prefetch unit being operable to receive from the memory simultaneously a plurality of prefetched instructions from sequential addresses in memory, and being operable to detect whether any of those prefetched instructions are an instruction flow changing instruction, and based thereon to output a fetch address for a next instruction to be prefetched by the prefetch unit, the prefetch unit comprising:

address generation logic ~~operable~~, ~~for~~responsive to a selected prefetched instruction that is detected to be said instruction flow changing instruction, ~~to determine~~for determining a target address to be output as the fetch address, the address generation logic having a first address generation path ~~operable to determine~~for determining the target address if the selected prefetched instruction is a first prefetched instruction in said plurality, and at least one further address generation path ~~operable to determine~~for determining the target address if the selected prefetched instruction is one of the other prefetched instructions in said plurality, the first prefetched instruction being earlier in said stream than said other prefetched instructions, the first address generation path ~~being arranged to generate~~generating the target address more quickly than the at least one ~~other~~further address generation path; and

a pipeline stage, provided in said at least one further address generation path, for increasing generation speed of the target address by the first address generation path, whereby, in the event that the first prefetched instruction is said selected prefetched instruction, the prefetch unit ~~is operable to~~ outputs the associated target address as the fetch address earlier than if one of said other prefetched instructions is said selected prefetched instruction.